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ClearSpeed Delivers Highest to Date Compute Density for Real Science at Supercomputing '07
Demonstrating the ClearSpeed Accelerated TeraScale System, new software tools, along with new partnerships and launching a Developer Community as HPC acceleration becomes mainstream

Supercomputing '07 (SC07) - Reno, NV – November 13, 2007 – ClearSpeed Technology (LSE:CSD), the world leader in acceleration for high performance computing (HPC), today announced the ClearSpeed Accelerated Terascale System (CATS). This small format system, taking up just 1U in a standard server rack, delivers up to one TeraFLOP of performance, achieving the world's highest ever compute density to date.

At the conference, ClearSpeed is demonstrating 12 CATS, each connected to an HP Proliant DL360 capable of delivering more than 11 TeraFLOPS double precision performance in a single rack and achieving new science conducted by Bristol University on the Influenza Virus. CATS are expected to halve the cost of modeling for scientific research at the molecular level, helping to broaden areas of new science. Later versions of CATS are intended to expand this impact even further.

The demonstration of CATS with HP coincides with ClearSpeed and HP announcements that ClearSpeed's Advance™ e620 accelerator cards have been adopted as a key feature of HP's HPC Accelerator Program. ClearSpeed's cards are the only accelerator technology approved for HP BladeSystem servers.

Leading up to today's announcement, ClearSpeed has also proven substantial increases in the number of applications which can now exploit ClearSpeed's acceleration. The expanded applications for real science include Molpro, Bristol University Docking Engine (BUDE), and Amber Implicit.

Alongside the expanded applications range, ClearSpeed is demonstrating its latest generation software release 3.0 Beta 1 which enables programmers to efficiently exploit the performance of ClearSpeed's acceleration. New features include improvements to the optimizing compiler intended to provide significant performance improvements for Cⁿ programs, a wider range of BLAS and LAPACK functions, expanded operating system compatibility to include Red Hat® Enterprise Linux® 5 64-bit and Suse® Linux Enterprise (SLES) Server 10 64-bit, improved use of on-chip memory, new library functions, and a number of improvements that further the ease of use capability. Additionally, a preview (Alpha) of the Eclipse integrated development environment (IDE) is available with the 3.0 Beta 1 release.

As a result of ClearSpeed's partnerships, its applications, and its product range, the ClearSpeed Developer Community was launched at SC07 with a successful first inaugural User Group held on Nov 12. The purpose of the developer community is to provide a forum for the expanding network of programmers exploiting ClearSpeed's technology. At the ClearSpeed User Group, presenters from a wide range of industries gave multiple sessions sharing their experience of working with ClearSpeed's acceleration.

“With so many key developments being announced with our partners at SC07 it is evident that for the first time acceleration is now becoming available for mainstream high performance computing,” said Tom Beese, ClearSpeed chief executive officer. “We are delighted with our partners and with fulfilling the promise of real performance for real science and real applications across multiple industries.”

About ClearSpeed

ClearSpeed Technology is a semiconductor company that develops massively parallel coprocessors and accelerator boards delivering unmatched performance per watt for high performance computing applications on industry standard systems. ClearSpeed has offices in San Jose, California and Bristol, UK and has over 50 patents granted with additional pending. For more information, visit www.clearspeed.com.