

*ClearSpeed*TM

The fastest solution for
credit risk analysis

world's fastest Monte Carlo engine

ClearSpeed's financial services industry benefits

- **Fastest 64-bit Performance**

- ClearSpeed's products deliver the highest 64-bit floating point performance, the standard required by the FSI industry

- **Highest Reliability**

- ClearSpeed's products include enterprise-class reliability features in hardware, unlike GPUs and FPGAs

- **Most Compute Density**

- ClearSpeed focuses on delivering the highest performance within the smallest space to maximize datacenter compute density

- **Greatest Energy Efficiency**

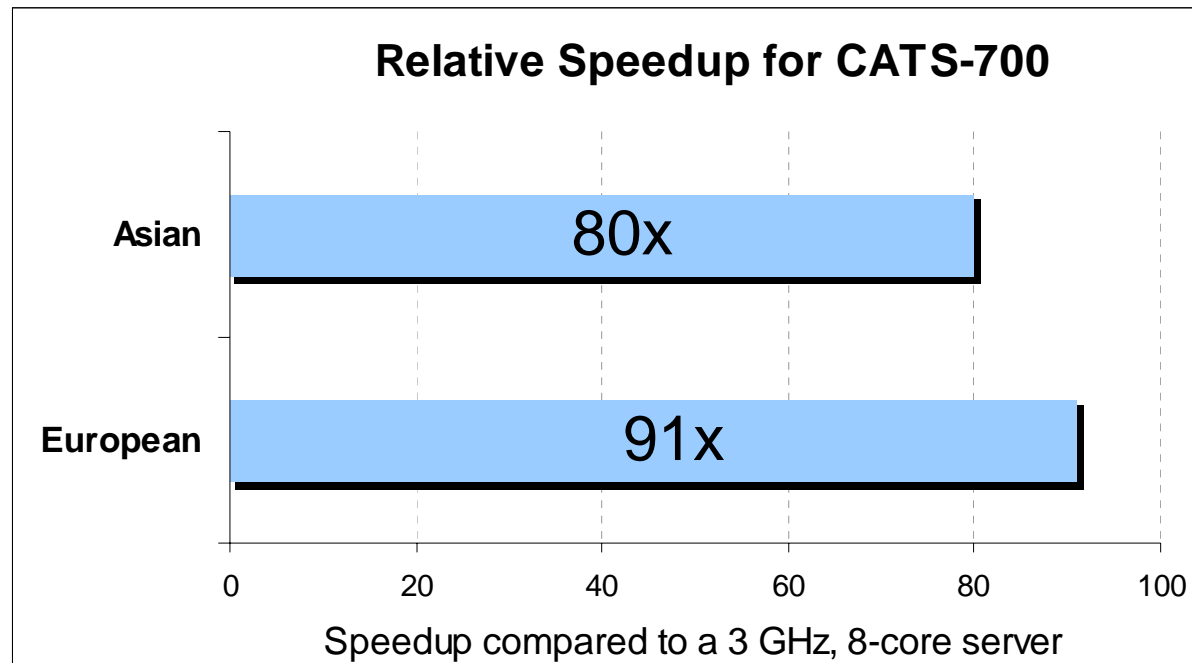
- ClearSpeed focuses on delivering the highest performance at the lowest energy consumption to fit within standard infrastructure power supply and cooling constraints

CATS-700 – 1.152 TFLOPS 64-bit in 1U for 300W



- 1.152 TFLOPS double precision (64-bit) in 1U
- Enterprise-class reliability designed-in (ECC etc)
- Only 300 watts typical power consumption for FSI
- 24 GBytes of DDR2 DRAM @ 96 GBytes/s
- *Up to 48 TFLOPS double precision in a single rack*
 - From 42 CATS-700 1U nodes

CATS-700 credit risk analysis performance



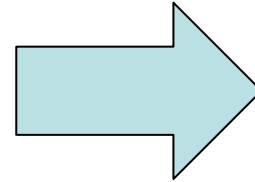
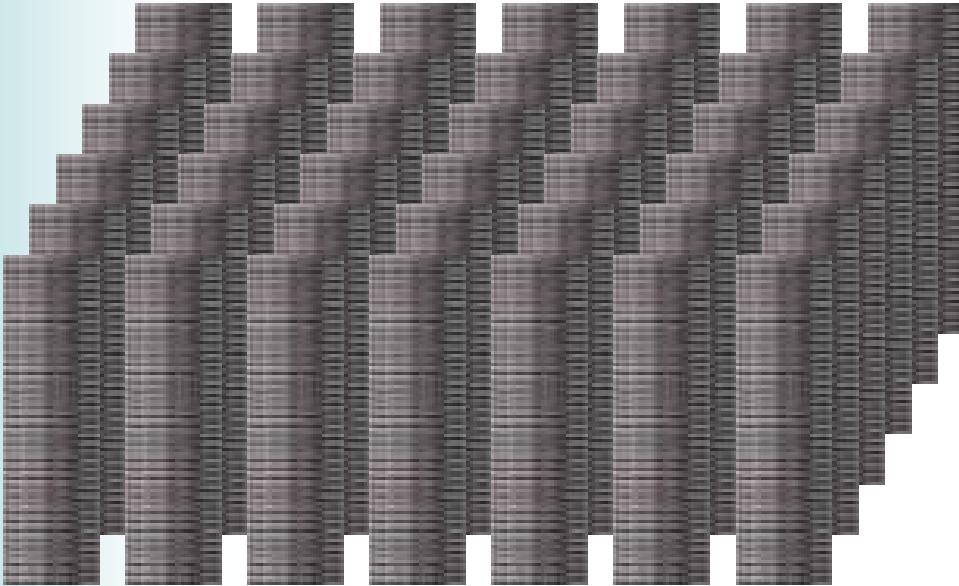
Comparing 64-bit Monte Carlo codes. Host code fully optimized with Intel's compiler and running on the latest 3GHz 8-core servers.

FSI customer success story

- A tier one Japanese bank chose ClearSpeed to accelerate their Monte Carlo-based credit risk analysis application
- Their application evaluates portfolios with tens of thousands of instruments across a large number of scenarios
- The application originally took 50 hours to run on a desktop machine
- After working with ClearSpeed for a few weeks the application ran in just 10 minutes on a CATS-700
- ***300X speedup for the customer on 64-bit code!***

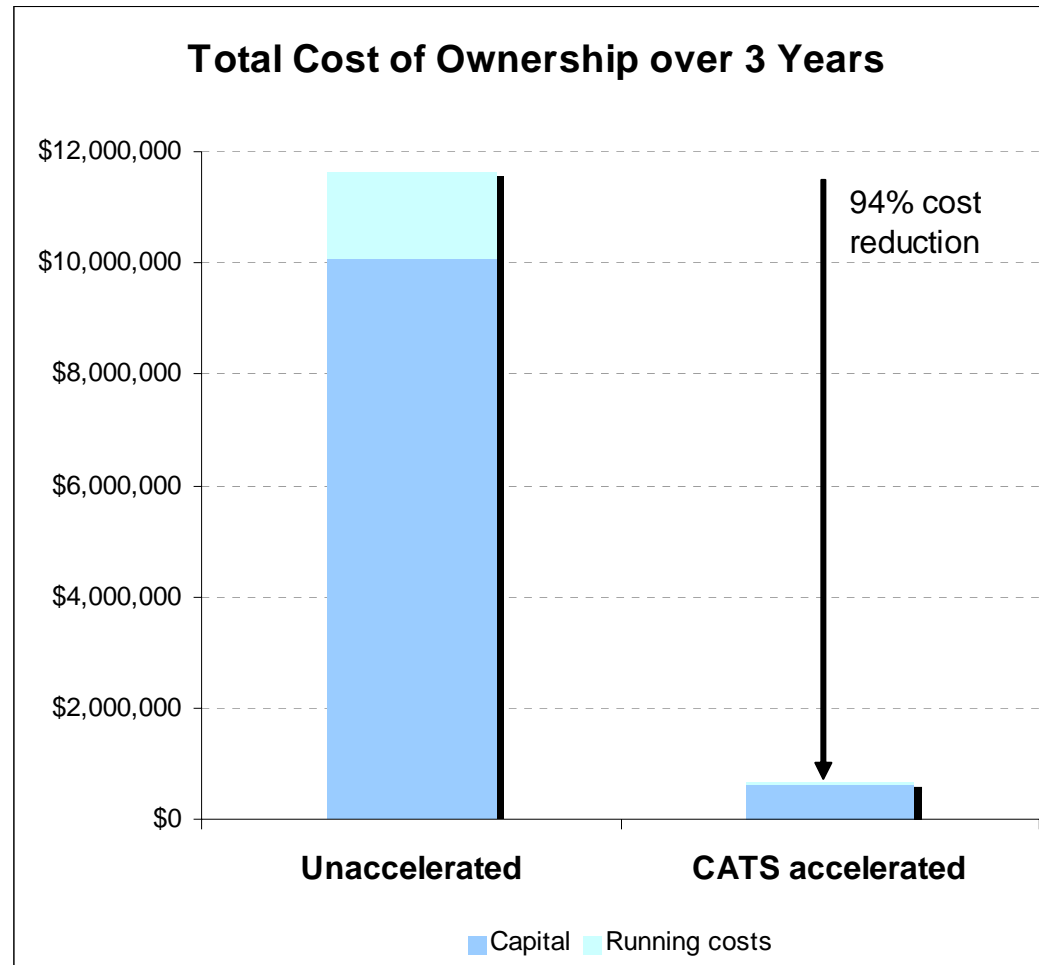
CATS – a massive leap forwards in compute density

- A single 42U rack filled half with CATS-700 and half with standard x86 servers delivers the same performance as over **40** racks of servers alone!



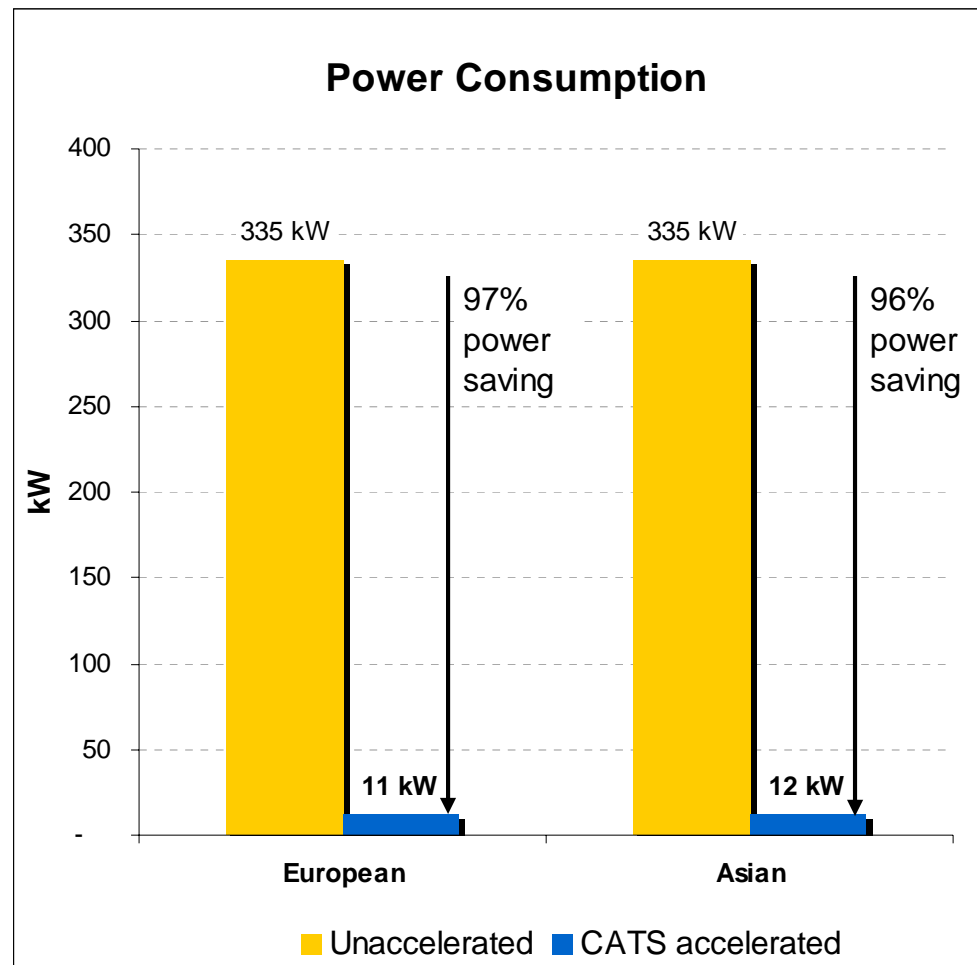
CATS – a massive reduction in costs

- Consolidating 40 racks of ordinary servers into a single CATS-700 accelerated rack saves >\$9.4M initial capital outlay and ~\$11M in TCO over 3 years



CATS – a massive reduction in energy consumption

- Consolidating 40 racks of ordinary servers into a single CATS-700 accelerated rack saves >96% in energy costs and CO₂ emissions



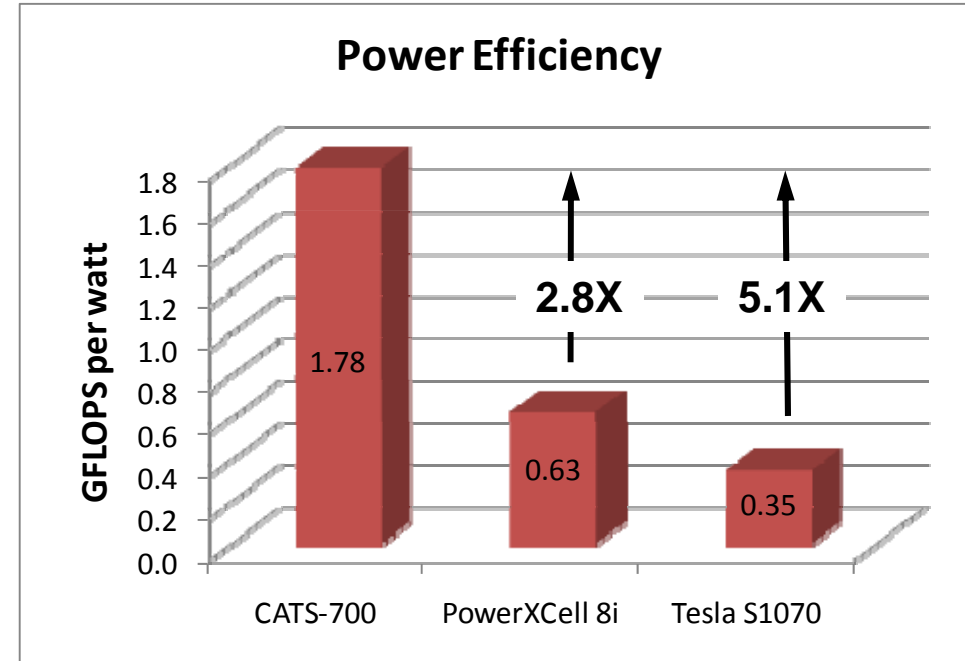
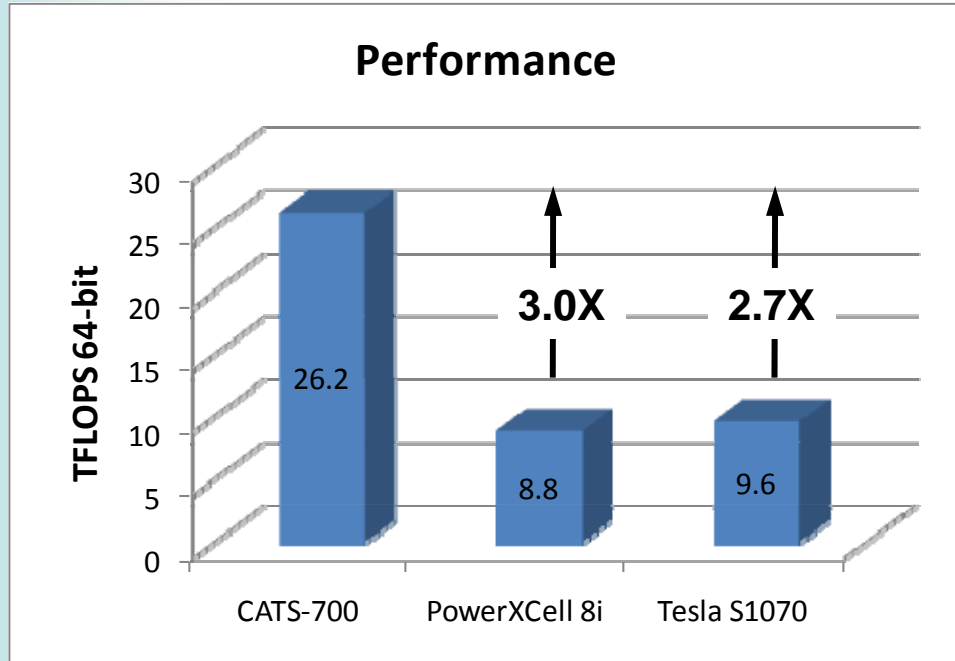
CATS-700 – a massive increase in reliability

- Consolidating 40 racks of ordinary servers into a single CATS-700 accelerated rack significantly improves system reliability
- CATS-700 has enterprise-class reliability designed-in:
 - E.g. all memories are protected from data corruption by Error Correcting Code (ECC) hardware mechanisms
 - E.g. its low power, cool design significantly improves MTBF
- CATS-700 based systems are much more reliable than GPUs
 - GPUs lack any reliability features in their hardware
 - GPUs silently deliver unreliable results
 - GPUs deliver unreproducible results
 - GPUs will crash much more often
- Bottom line: GPUs simply will not work for FSI



CATS-700 – The fastest accelerator for FSI

Consider a standard 42U rack filled half with accelerators and half with the latest 3GHz, 8-core x86 servers:



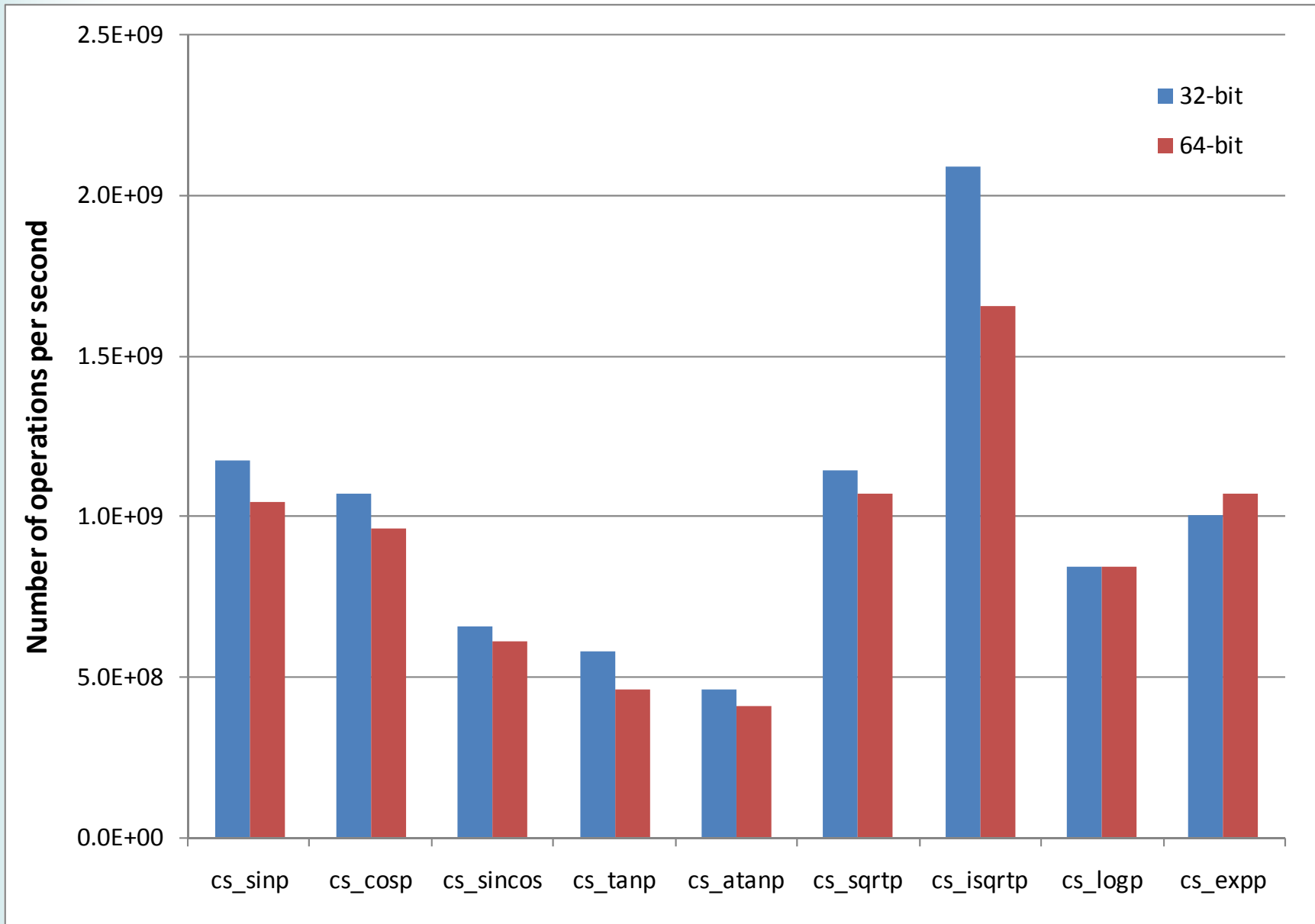
CATS-700 accelerated systems deliver far more performance and compute density than *all* other solutions on the market

A PetaFLOP of CATS



- Just 50 racks!
- Enterprise-class *reliable* PetaFLOP
- 1.125 PFLOPS double precision of CATS-700
 - Additional 90 TFLOPS double precision from x86 hosts
- 630KW typical power consumption for FSI applications

CATS-700 transcendental function performance



Powerful software development environment

- ClearSpeed's CATS accelerators are programmed in a version of ANSI C with language extensions to support vector data types
- The Software Development Kit is very mature:
 - Based on the CoSy commercial compiler from ACE
 - ClearSpeed's SDK is now in its 3rd release
- Debugger based on the industry standard GDB
- Best in class profiler with heterogeneous, system-wide capabilities
- Example FSI codes in source code form
- Libraries of optimized Random Number Generators, also available in source code form
- ECLIPSE-based IDE



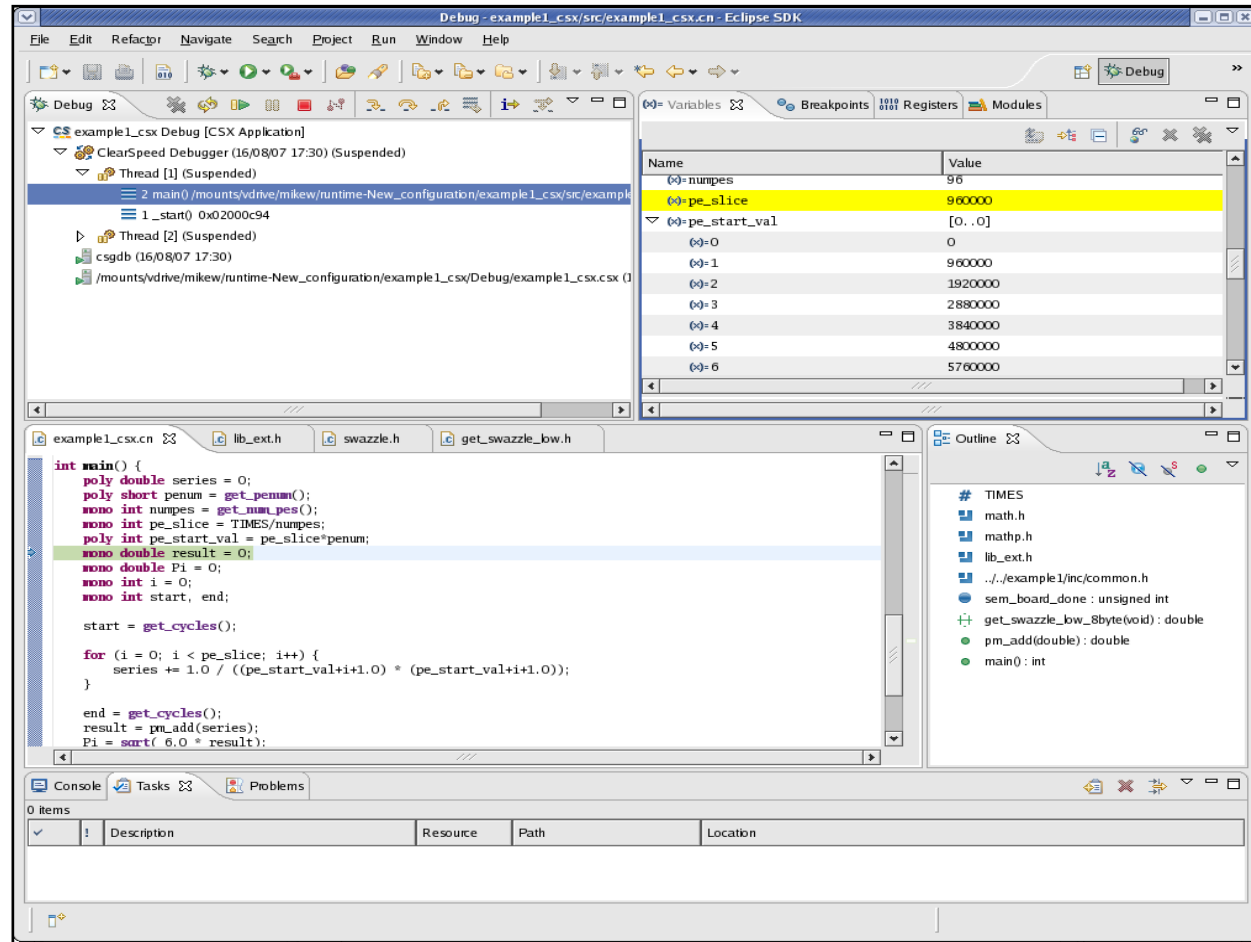
Debugging CATS with the industry standard IDE



Standard Eclipse graphical debug interface for CATS processor debugging.

CATS' processors support full hardware debugging of application code.

Provides a seamless view of many processor cores in parallel.

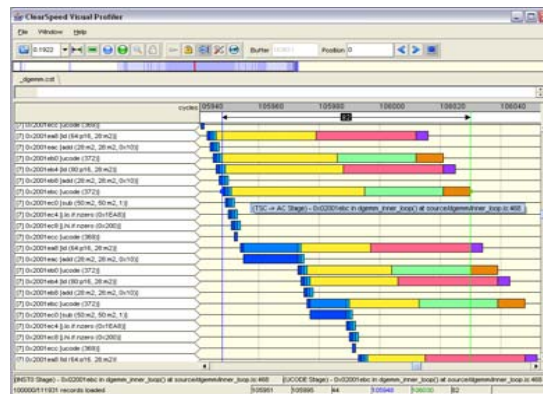
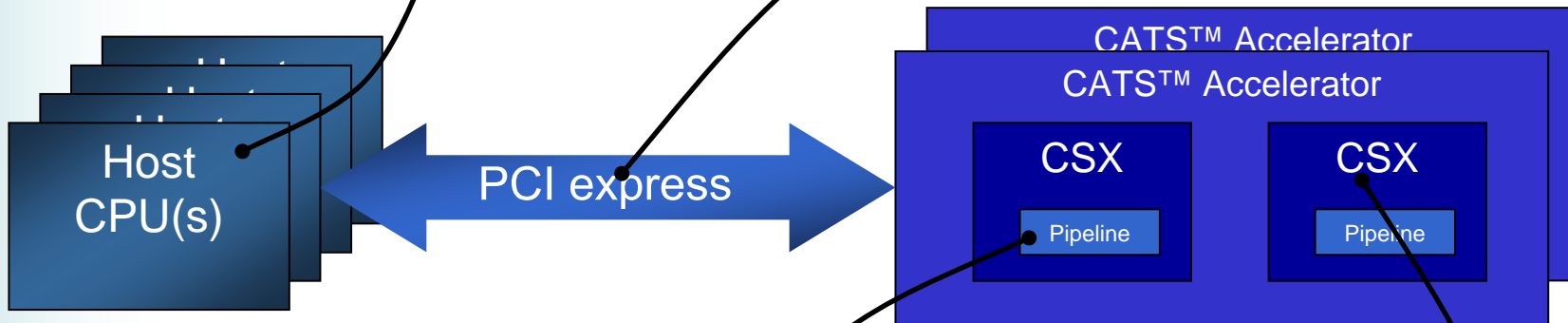
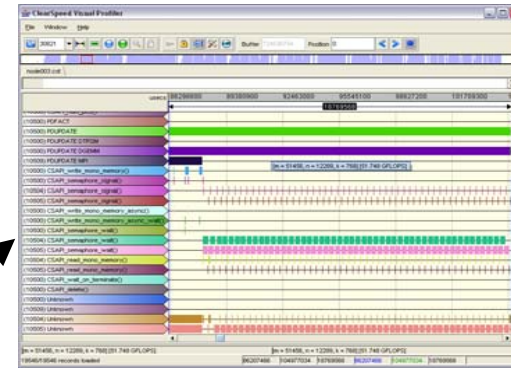


Best-in-class profiler for accelerators

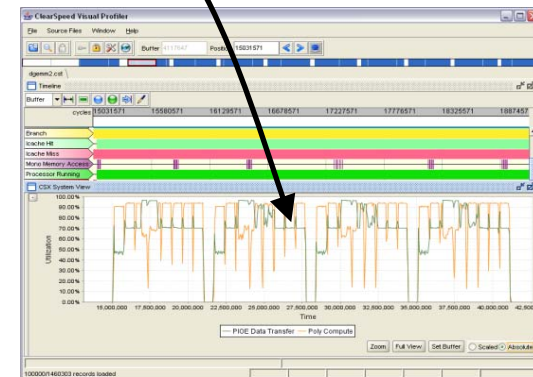
HOST CODE PROFILING



HOST/CATS INTERACTION PROFILING



CSX PIPELINE PROFILING



CSX SYSTEM PROFILING