



ClearSpeed Technology

Performance Processors

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- **SKA Processing**
 - Performance requirements
 - Technology comparison
 - Use of SIMD in an ASIC device

- **ClearSpeed's technology**
 - Hardware IP
 - Software tools
 - Design services

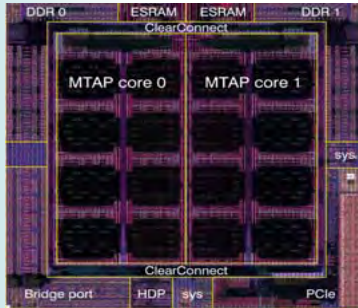
Company overview

- **ClearSpeed Technology formed in 2002**
- **Architecturally Low power / High Performance**
- **Highest efficiency processor technology**
 - Supported by SDK, libraries and applications
- **Ultra-high performance processing to enhance DSP / Embedded Solutions**
 - Automotive, Mil/Aero, Pro-Audio, Image Processing
- **Circa 100 patents applied for or granted on the technology**



- **Available as an IC in BGA package**
- or
- **Licensable IP**
 - Processor cores
 - High bandwidth interconnect fabric
 - Network on chip
 - Fully Scalable

Products



Chips and IP

- CSX700 processor
 - 10 GFLOPS/Watt double precision
- Multi-threaded enhanced SIMD
 - Low power, High performance
- Easy to Use
 - SDK allows programming in C
 - HDK allows easy integration
- Reliable – Error Checking and Correction (ECC) on all memory
- Robust – Multi-level redundancy makes the design suitable for use in harsh environments
- Also available as IP

Boards

- e710, e720 cards
- 150 GFLOPS 64 bit
- Single slot PCI Express x8
- Software support for multiple boards
- 2 GBytes of ECC protected DRAM
- 32/64-bit drivers for Windows and Linux
- 30 watts maximum for entire board
- Available Now



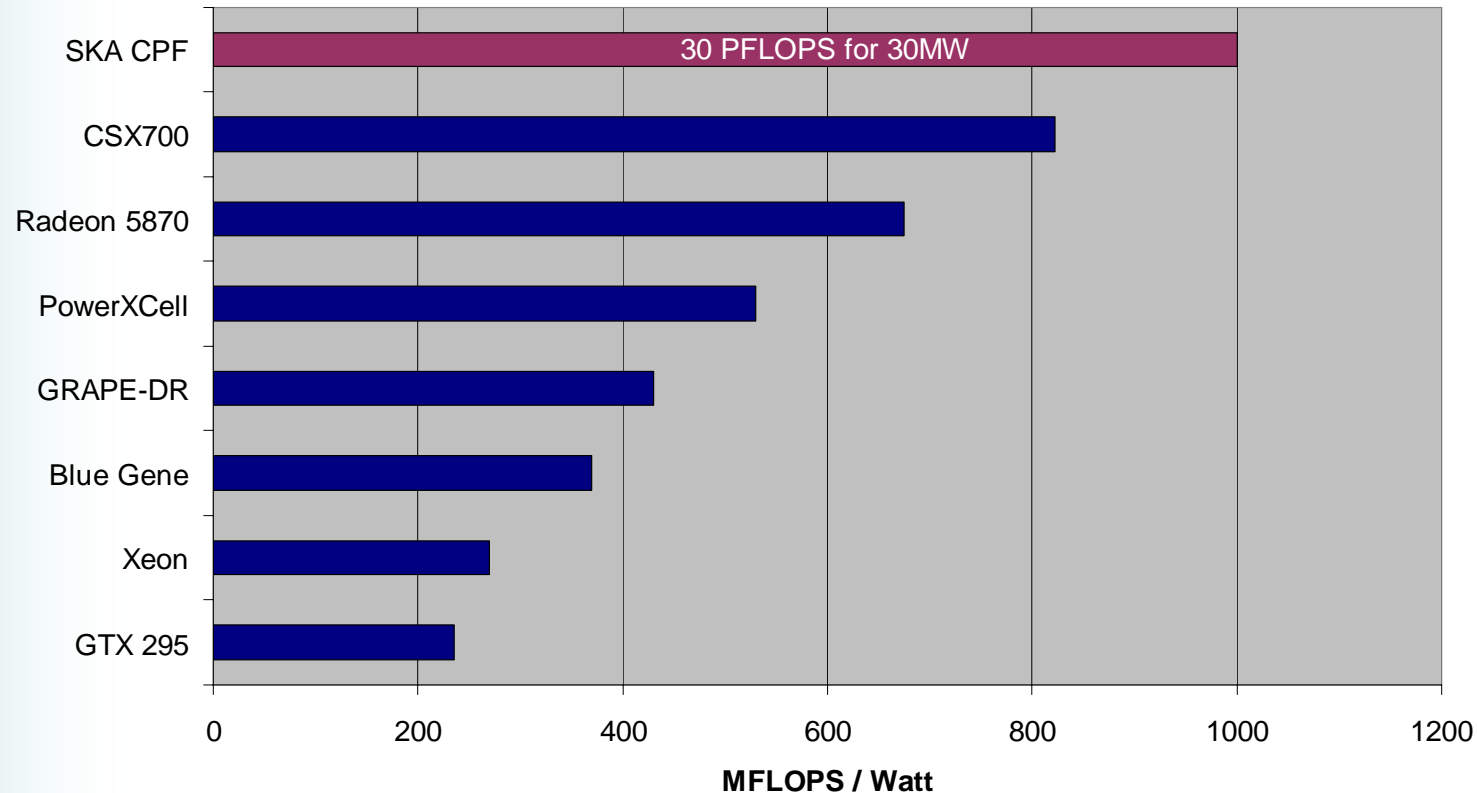
Systems

- CATS-700 - 1U rack accelerator
- 1.8 TFLOPS (32 and 64-bit)
- 400 watts typical power
- *72 TFLOPS 64-bit in a single rack*
- Low power and portable systems also in development



SKA Post processor performance

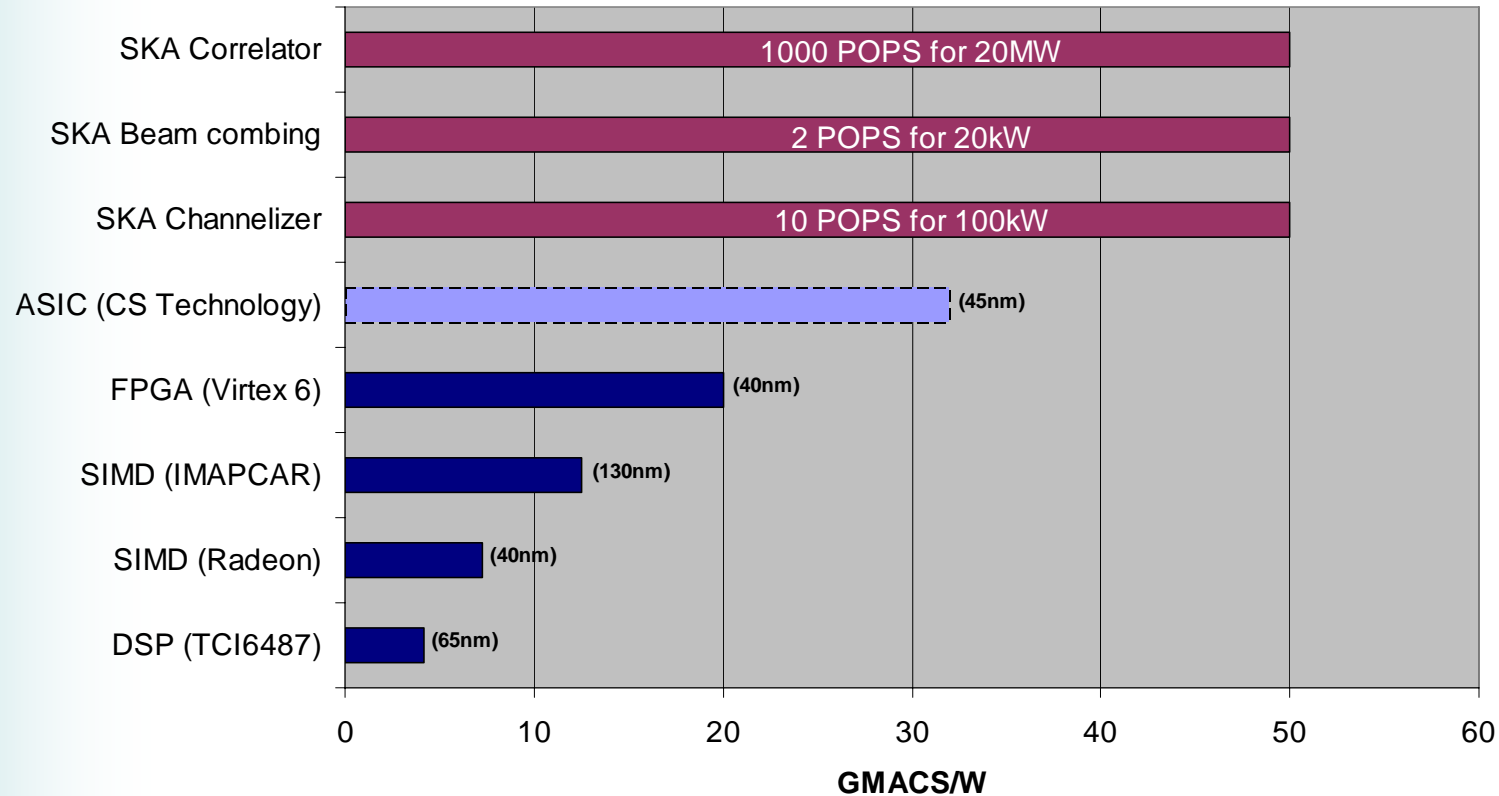
Linpack system performance



- **Post processing requirement in the Central Processing Facility**
 - **Almost met by existing SIMD processors (ClearSpeed, GPGPU)**
 - **Only a factor of two or three times above existing super computers**

AA Station Processors and Correlator

Fixed point processor performance



- **Fixed point processing requirements**
 - **Only a factor of two or three times above existing technology**
 - **Most likely to be met with an ASIC or FPGA**

Technology comparison

	Advantages	Disadvantages
ASIC	<ul style="list-style-type: none">• Optimum performance• Low power• Devices are low cost	<ul style="list-style-type: none">• Significant investment (\$10M)• Fixed function
FPGA	<ul style="list-style-type: none">• Optimum performance• Reconfigurable• Algorithms developed	<ul style="list-style-type: none">• Expensive to develop• Devices are expensive
SIMD	<ul style="list-style-type: none">• Software programmable• Low power• Devices are inexpensive	<ul style="list-style-type: none">• Hardware not optimised
DSP	<ul style="list-style-type: none">• Software programmable• Easy to program	<ul style="list-style-type: none">• Hardware not optimised• Lacks performance per Watt

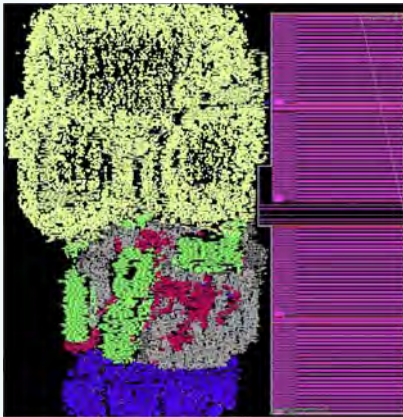
ASIC features for SKA

- Integrated ADCs (128 channels on CMOS)
 - 1GS/s 6bit flash ADC on 90nm CMOS for 72mW per channel
- Buffers suitable for largest FFT in channelizer
- Configurable processor optimised for
 - Fixed point, Complex arithmetic
 - FFT and / or Digital Down Conversion in channelizer
 - FFT or DFT in beam combing
- High performance (8 Tera OPS, fixed point for 80W)
- High bandwidth interconnect
- High bandwidth interface to correlator

SIMD features for SKA

- Processing Elements optimised for
 - Fixed point, Complex arithmetic
 - FFT and Digital Down Conversion
 - Number of Adders, Multipliers and Registers
- Suitable interconnect between Processing Elements
- Memory suitable for largest FFTs

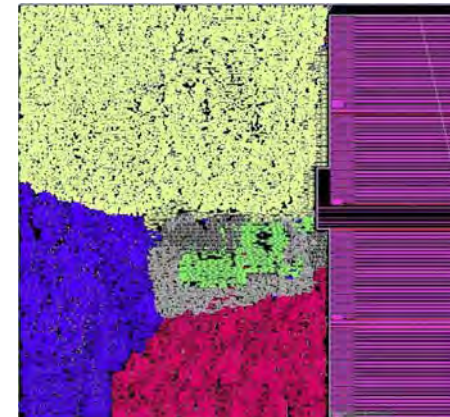
Fixed point 32bit



45nm (Not optimised)

Red: Adder
Blue: Multiplier
Yellow: Register file
(256 byte 6 port)
Purple: Memory (6KB)

Floating point 32bit



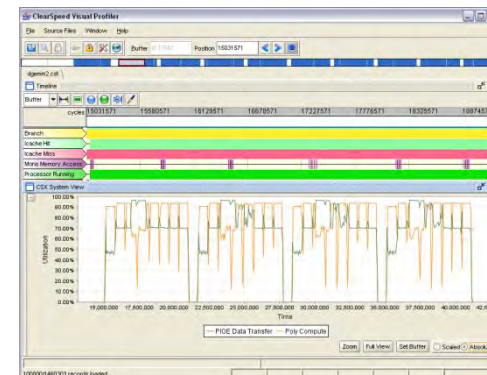
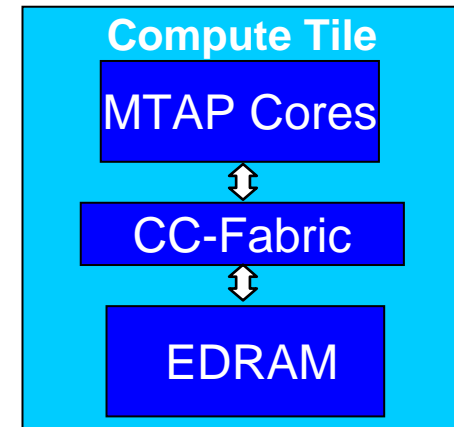
TECHNOLOGY

Hardware IP

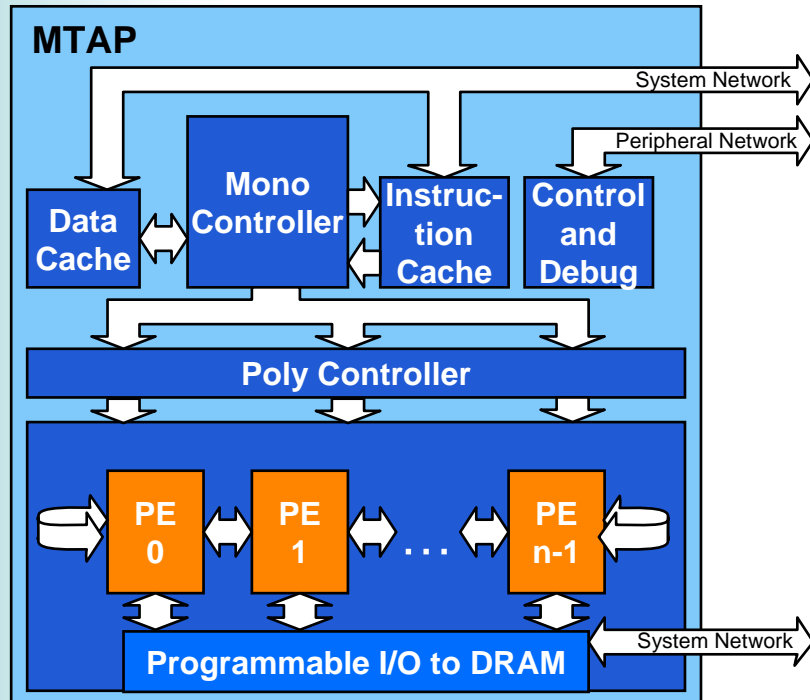
- **MTAP** - High efficiency multi-threaded enhanced SIMD processor
- **ClearConnect** - High bandwidth fabric and network on chip
- All silicon design captured in Verilog RTL
- Fully scalable

Software Technology

- State of the Art visual profiler for heterogeneous multi-core systems
- Platform independent

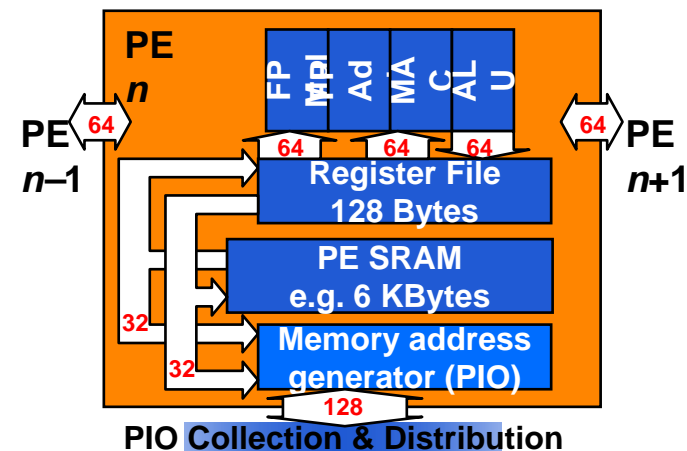


IP - MTAP processor core



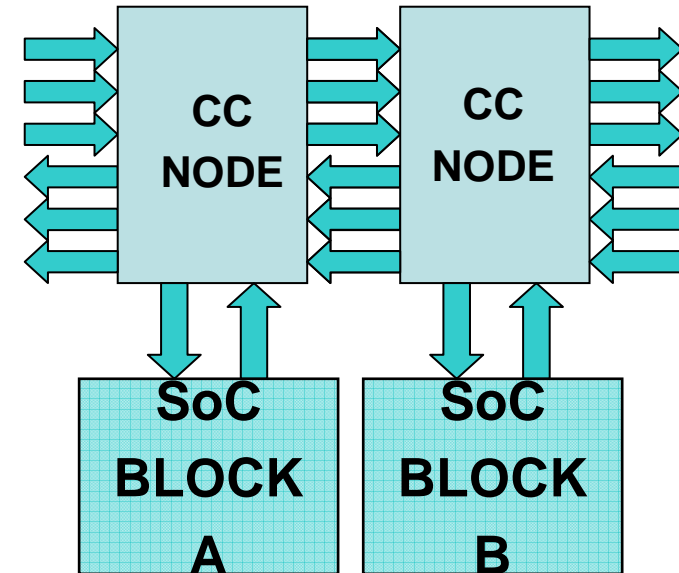
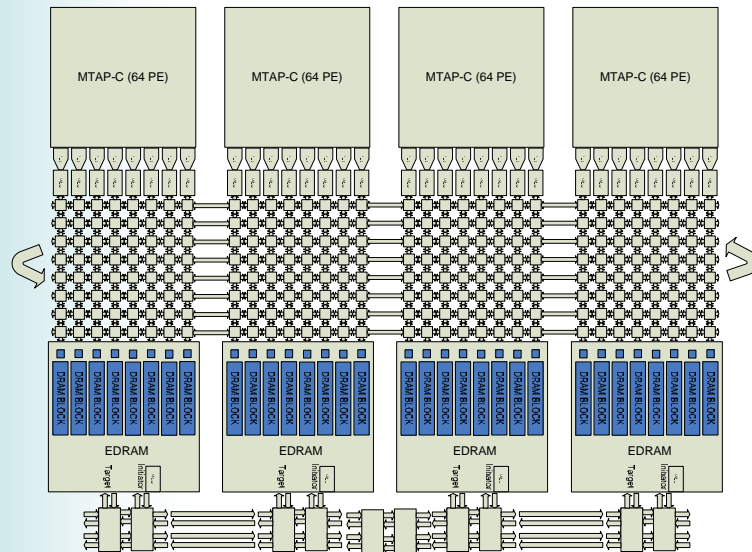
- Smart SIMD Multi-Threaded Array Processor
- Designed for high performance and low power
- Multi-threading enables asynchronous, overlapped I/O with compute
- Programmed in an extended version of ANSI C called Cn – adds variable type ‘poly’

- Configurable number of processing elements
- 32 and/or 64 bit systems possible
- Single or Multi-MTAP SOC's easy to implement



IP – ClearConnect High-Bandwidth Interconnect

- Scalable, System on Chip interconnect
- “Network-on-a-chip” forms System backbone
- Used to connect together all the major blocks on a chip e.g. MTAPs, other processor cores, memory controllers, system interfaces etc
- Blocks are connected into a unified memory architecture



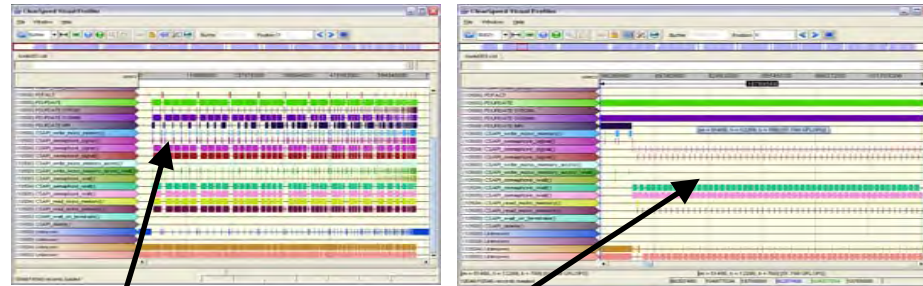
- Distributed arbitration
- Scalable bandwidths
- Low power - dissipation is proportional to volume of data and distance travelled
- Can be used to form High Bandwidth fabric to connect processing elements to embedded DRAM for example

Technology - profiler for heterogeneous multi-processor systems

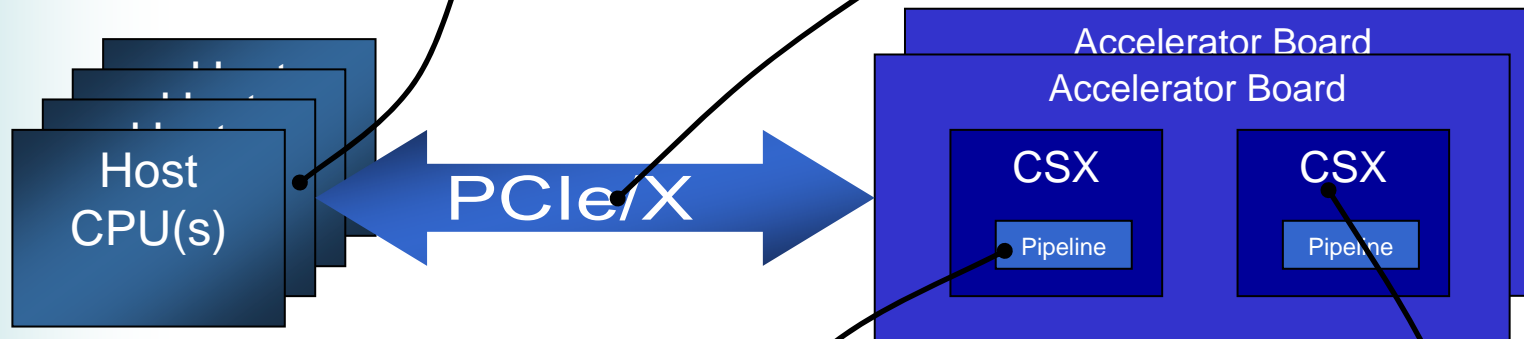
- **Processor agnostic, state of the art heterogeneous profiler for optimising software on multi processor systems**

HOST CODE PROFILING

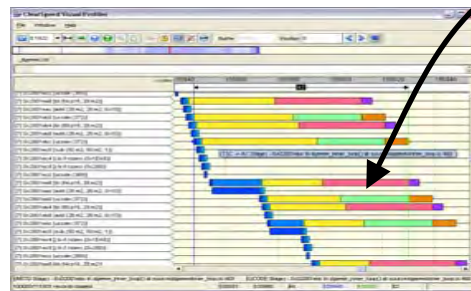
Visually inspect host code executing. Shows execution of multiple threads



INTERACTIONS - Provides performance information and overlap for interactions between processors



PIPELINES - Visualize detailed instruction issue, timing and overlap of executing instructions for optimisation

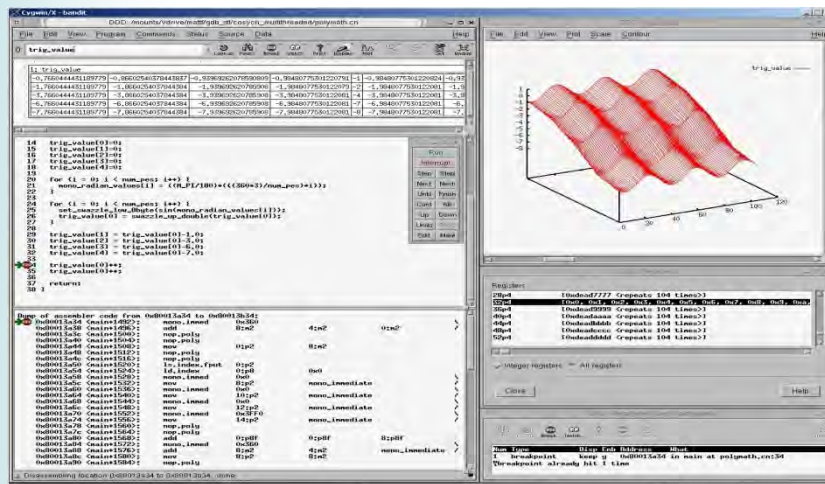


SYSTEM LEVEL - Visualize the compute - I/O overlap, and cache utilization. View branch trace of code executing and get accurate event timing for optimisation



ClearSpeed software development environment

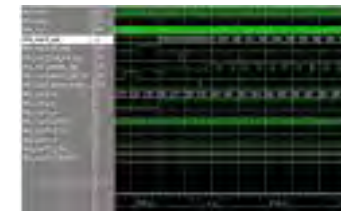
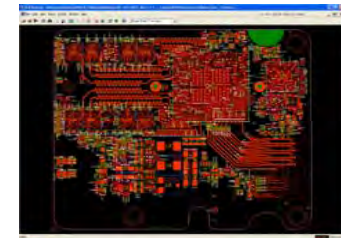
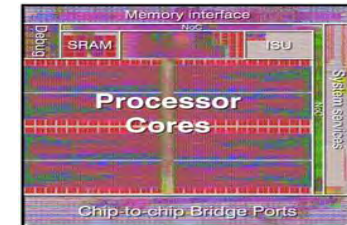
- The SDK includes:
 - Sophisticated C compiler with support for parallel data types
 - Advanced, heterogeneous profiler for analyzing multi-processor, system-level performance
 - Open source debugger based on the industry standard GDB



- Developer libraries delivered in *both* binary and source code form, including FFTs, random number generators, matrix operations (BLAS)
- Drivers for Linux (open source) and Windows
- High-quality documentation and training material

Design Services

- **Rapid prototyping**
- **Concurrent design**
- **In-house automation tools for ensuring functional interface consistency and verification**
- **In-house verification systems for quality assurance**
- **In-house automation for physical implementation**
- **State of the art verification methodology to ensure 'right first time' design**
- **Custom drivers and software tools**



- **ClearSpeed provide Post-Processing hardware today**
 - Low power SIMD hardware for use in HPC
 - Visit <http://www.clearspeed.com>

- **ClearSpeed's technology approaches the SKA fixed point processing requirements**
 - Low power ASIC using enhanced SIMD IP
 - Use of SIMD technology in an ASIC combines the advantages of optimised hardware and software programmability
 - SIMD algorithms can be developed on today's hardware

- **ClearSpeed provides**
 - Low power hardware IP
 - Software tools
 - Design services

ClearSpeed™

ClearSpeed



ClearSpeed™

The future of high efficiency processing

For processor IP, silicon, boards, software and design services

Contact: **enquiries@clearspeed.com**

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